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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,889	08/09/2006	Henricus Hubertus Van Den Berg	NL04 0134 US1	4101

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/588,889	VAN DEN BERG ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/9/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is required to provide appropriately located section headings to be used in the specification (see guidelines for the arrangement of specification below).

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Drawings

The drawings are objected to because suitable meaningful literal legends are required for the numerous empty boxes in figures 1,2,3,4,5,6 (see Rule 1.84(o)). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 13 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 13 is directed to a computer program product with instructions… . However the computer program product is not stored in a computer readable storage medium . Therefore the program product is not embodied in a manner so as to be executable. Therefore claim 13 is directed toward non-statutory subject matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 8-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Early (patent No. 7,299,307).

Early taught the invention as claimed including a data processing ("DP") system comprising(as per claim 1): an array of interconnected and programmed or programmable digital signal processors (110,120), at least some of the digital signal processors having IO ports (102),(e.g., see fig. 1); an IO connection for communicating a signal stream between signal processor in the array and circuitry outside the

array(e.g., see fig. 1); a configurable multiplexing circuit (103) between IO connection and the IO ports of at least a plurality of digital signal processors the multiplexing circuit being configurable under control of configuration data, the multiplexing circuit being arranged to give the effect of accessing the IO connection only to IO signals from the IO port or port of one or ones of the respective plurality of digital signal processors that are selected by the configuration data (e.g., see col. 4 line 44-col. 5, line 26 and figs. 1 and 3, and col. 6 line 62-col. 7, line 6).

As to claim 2, Early taught the multiplexing circuit is arranged to give unconditional, arbitration free access from the IO port of the selected one or ones of the plurality of digital signal processors to the IO connection (e.g., see fig.1)[the multiplexing circuits are arranged in parallel].

As to claim 3, Early taught a plurality of IO connections including IO connection and a plurality of configurable multiplexing circuits including the configurable multiplexing circuit, each configurable multiplexing circuit coupling a respective IO connection to IO ports of at least a respective plurality of digital signal processors, each multiplexing circuit being arranged to give the effect of accessing the IO connection only to IO signals from the IO port or ports of one or ones of the respective plurality of digital signal processors that are selected by the configuration data for that multiplexing circuit the IO port of at least one of the digital signal processors being coupled in common to a plurality of the multiplexing circuits separately from the IO ports of other digital signal processors(e.g., see fig.1)[the digital signal processors are coupled via an external bus in common to plural multiplexing circuits separately from I/O

ports of other digital signal processors such as the processor coupled to input connections].

As per claim 4, Early taught a peripheral coupled to a respective one of the IO connections the peripheral circuit having a control input, the peripheral circuit being responsive to respective control signal values at the control signal values at the control input the IO signal selected under control of the configuration data the multiplexing circuit being arranged to translate the IO signals from the IO ports of the selected one or ones of the signal processors into respective control signal values associated with the IO signal values for supply for the peripheral circuit (e.g., see fig. 6 and col. 8, lines 34-63).

As to claim 5 Early taught the multiplexing circuit is arranged to associate a control signal value with respective, independently configurable IO signal values from different ones of the respective digital signal processors respectively(e.g,. see fig. 1)[multiplexers characteristically comprise control signal input, and in figure 1 the Early system arranged the multiplexers in parallel which provides for independently configurable IO signals from different digital signal processors] .

As per claim 8, Early taught the configuration data of the multiplexing circuits is programmable under control of signals from the IO ports of the digital signal processors (e.g., see col. 4, line 59-col. 5, line 14 and col.6, line 63-col. 7, line 6).

As per claim 9, Early taught the digital signal processors are programmed to perform a signal processing operation that comprises a plurality of tasks, each task executed by a respective one of the digital signal processors the integrated circuit

comprising neighbor interconnections between digital signal processing circuits in the array (e.g., see col. 5, lines 15-48, and col. 6, lines 37-61), in which signal processing operation signal streams flow between respective tasks from an to IO connections and to front end and/or from back end task of said task via the IO connections respectively(e.g., see fig. 1 and col. 4, line 44-col. 5, line 15), and wherein the digital signal processing integrated circuit is programmed to establish a configuration wherein the multiplexing circuits are configured so that only IO signals from the IO ports of one or ones of the respective plurality of digital signal processors that execute the front end and / or back end tasks have the effect of accessing the respective IO connections (e.g., see fig. 1) [the connections to some multiplexers provide input to DSPs in parallel and the ouput bus is connected to other multiplexers for providing output in parallel]..

As to claim 10, Early taught the signal processor that executes a particular front end and/or back end task is programmed to write the configuration data to the multiplexing circuits to establish a configuration wherein the multiplexing circuits access the IO connection with which the front end and/or back end task exchanges the signal streams in response to IO signals from that particular digital signal processor (e.g., see col. 7, lines 1-6).

As per claim 11, Early taught a method of executing a signal processing operation that inputs and/or outputs a stream of signal data, the method comprising the steps of executing different tasks that are part of the signal processing operation by executing respective programs in respective digital signal processors in an integrated

circuit, communicating intermediate streams of data between tasks in different signal processors (e.g., see col. 6 lines 37-61) the digital signal processors including a particular digital signal processor that executes a front end and/ or back end task that contains an IO instruction for receiving and/or transmitting signal from an external stream of signal data (e.g., see col. 3, line 62-col. 7, line 16); prior to said executing, programming configuration data of a multiplexing circuit (e.g., see fig. 3)that is coupled between an IO connection and IO ports of at least a plurality of digital signal processors the configuration data(e.g., see fig. 1) controlling the multiplexing circuit to give the effect of accessing the respective IO connection only to IO signals from the IO port of the particular digital signal processors that are selected by the configuration data (e.g., see col. 4, line 59-col. 5, line 14).

As to claim 12, Early taught a switch between the programmed signal processing operation is executed, the switch comprising reprogramming the configuration data so that mutually different ones of the digital signal processors execute the front end and/or end task before and after the switch (e.g., see co.. 1, lines 28-64 and col. 6,line 49-col. 7, line 6).

As to claim 13, Early taught a computer program product with instructions for executing a signal processing operation that inputs and/or outputs a stream of signal data, the instructions comprising instruction for executing the steps of: executing different tasks that are part of the signal processing operation by executing respective programs in respective digital signal processors in an integrated circuit, communicating

intermediate streams of data between tasks in different digital signal processors (e.g., see col. 6 lines 37-61) the digital signal processors including a particular digital signal processor that executes a front end and/ or back end task that contains an IO instruction for receiving and/ or transmitting signals from an external stream of signal data (e.g., see col. 3, line 62-col. 7, line 16); prior to said executing, programming configuration data of a multiplexing circuit (e.g., see fig, 3) that is coupled between an IO connection and IO ports of at least a plurality of the digital signal processors the configuration data (e.g., see fig. 1) controlling the multiplexing to give the effect of accessing the respective IO connection only to IO signals from the IO ports of the particular digital signal processors that are selected by the configuration data(e.g., see col. 4, line 59-col. 5, line 14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Early as applied to claims 1-5 above, and further in view of Yard (patent No. 5,892,934).

As to claim 6, Early taught the plural DSPs coupled to external I/O via multiplexers (e.g., see figs.1,3). Early did not specifically detail a I/O instruction. Yard however taught the digital signal processor is arranged to execute IO instruction that

specify IO address, the IO ports having address lines for outputting the IO address, the multiplexing circuit being arranged to configurably associate each selected digital signal processor that is connected to the multiplexing circuit (74) to a respective configurable IO address value (e.g., see col. 9, line 1-col. 10, line 67), the multiplexing circuit being arranged to enable transport of data between the respective processor in response to receiving from the IO port of the particular one of the signal processing circuits, the IO address value that is configurably associated with that particular one of the processing circuits (e.g, see col 11 ,line 1-col. 12 line 64) .

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Early and Yard. Both references were directed toward the problems of coupling DSPs to external I/O therefore one of ordinary skill would have been motivated to incorporate the Yard teachings of an I/O instruction and address comparators at least to provide efficient selection of connections between each DSPs and external I/O. Also the incorporation of the Yard teachings would have yielded predictable results.

As per claim 7, Early taught a plurality of configuration data storage. elements(e.g., see col. 7, lines 1-6), Yard taught a plurality of comparators each comparator (72) having a first input coupled to a respective one of the configuration data storage elements and a second input coupled to the IO port to a respective one of the digital signal processors for receiving IO addresses (e.g., see figs. 4,5,6 and col. 11, line 1-col. 12 line 64).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kopp (patent No. 5,450,557) disclosed a single chip self configurable parallel processor (e.g., see abstract).

Wester (patent No. 3,815,095) disclosed a general purpose array processor (e.g., see abstract).

Watts (patent No. 5,581,600) disclosed a system with plural DSPS connected via interface cards (e.g. see fig. 18).

Lawrie (patent No. 4,051,551) disclosed a multidimensional parallel access computer memory system with multiplexers controlling parallel access between processors and memory (e.g., see fig. 3 and abstract).

.Bright (patent No. 5,541,862) disclosed an emulator and digital signal analyzer (e.g., see abstract) and figs. 1, 2, 3).

Szymboski (patent No. 5,121,342) disclosed and apparatus for analyzing communication networks (e.g., see fig. 1 and abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

/Eric Coleman/
Primary Examiner, Art Unit 2183